GENLINX™ II
EB9025/20 Evaluation Board

PRELIMINARY

INTRODUCTION

The EB9025/20 is an evaluation and reference design platform for the ***GENLINX™ II*** GS9025 Receiver, the GS9020 Serial Digital Video Input Processor, and the GS9028 Cable Driver. The board performs the function of serial to parallel conversion and EDH processing for serial digital video signals. The board also provides a re-serialized, EDH compliant serial data output.

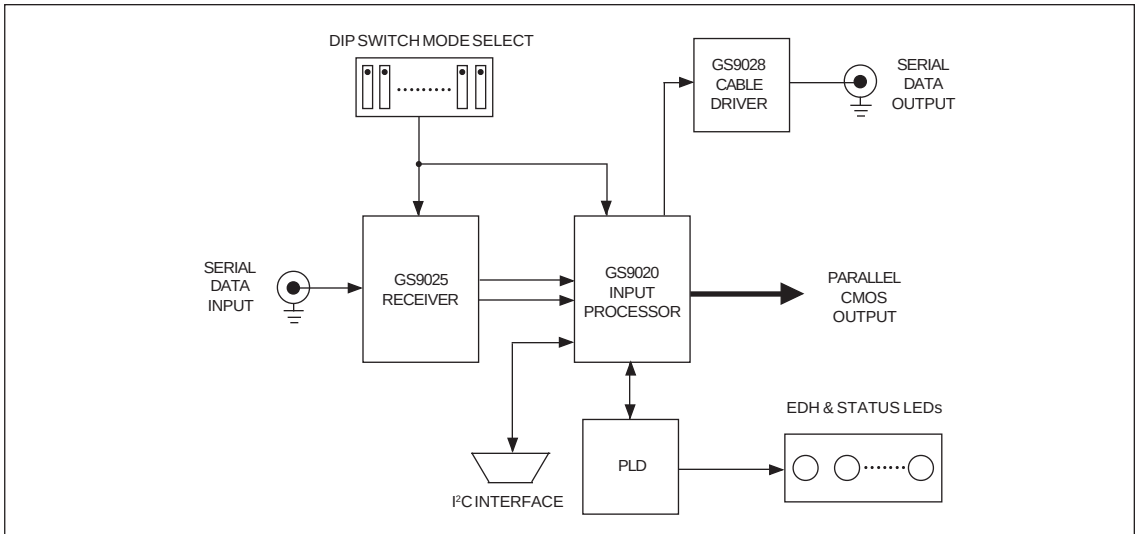
CIRCUIT DESCRIPTION

A block diagram of the board is shown below and illustrates the primary circuit functions. These include, equalization, reclocking and clock extraction in the GS9025, serial to parallel conversion and EDH and data processing in the GS9020, and redistribution of the reclocked and EDH compliant serial data through the GS9028. A full schematic is also included.

The incoming serial digital signal is connected via a BNC connector to the analog inputs of the GS9025. Equalization of the input signals is completely automatic for signal attenuation due to cable length from 0dB to in excess of 30dB. The signal strength/carrier detect output of the receiver, which is proportional to the amount of equalization taking place, is available via a test point. In addition, a LOCK LED is provided to visually indicate when the receiver has locked to the incoming video signal.

The GS9025 data and clock outputs are supplied to the GS9020 for serial to parallel conversion and EDH processing. The resulting decoded and EDH processed CMOS (TTL compatible) data is available through a 48 pin connector. A companion TTL to ECL converter module is available to provide ECL outputs through a DB25F connector conforming to bit-parallel standards (SMPTE 125M and SMPTE 244M). The EDH compliant data is also re-serialized and supplied to the GS9028 to provide a reclocked serial data output at BNC J1. The cable driver is configured to drive 75Ω co-axial cables. The STD[3:0], TRS_ERROR, and F[2:0] outputs of the GS9020 drive LEDs which visually indicate the incoming video standard, the occurrence of errors in the TRS words, and the current field. In addition, the INTERRUPT, FIFO_RESET, and NO_EDH output signals are available via test points.

A PLD is provided primarily to interface to the Flag Port of the GS9020 and extract the Ancillary, Full Field, and Active Picture error flags. The PLD is designed to cycle the S[1:0] inputs of the GS9020, read and demultiplex the output error flags, and drive the status LEDs providing visual indication of the type of EDH errors present. The PLD is also designed to control which error flags are read from the GS9020 Flag Port — incoming or outgoing. Upon power-up or RESET, the board is configured to display the outgoing EDH error flags. When the INC. FLAGS push-button is depressed, the PLD writes to the GS9020 flag port instructing it to output the incoming EDH error flags instead. To return to the outgoing error flags, the system must be RESET. Finally, the PLD is



EB9025/20 BLOCK DIAGRAM

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used to buffer the GS9020 field output signals and drive the field indicator LEDs.

A DB9F connector (J2) is provided for access to the I²C interface of the GS9020. I²Cslave address bits are set via DIP switch SW2. For a detailed description of the GS9020 I²C interface refer to the GS9020 data sheet.

Finally, three DIP switches are provided for configuration of the GS9025 and GS9020. A detailed description of the input and output pins of each device can be found in the respective data sheets.

BOARD SET-UP AND TEST

The board is configured in SMPTE, auto-tune mode and supports five data rates: 143Mb/s, 177Mb/s, 270Mb/s, 360Mb/s, and 540Mb/s. LED indicators are used to indicate when the device is LOCKed and the detected standard as shown below:

	STD2	STD1	STD0
NTSC 4:2:2 Component with 13.5 MHz Y sampling	0	0	0
NTSC Composite	0	0	1
NTSC 4:2:2 16x9 Widescreen with 18 MHz Y sampling	0	1	0
NTSC 4:4:4:4 Single Link with 13.5 MHz Y sampling	0	1	1
PAL 4:2:2 Component with 13.5 MHz Y sampling	1	0	0
PAL Composite	1	0	1
PAL 4:2:2 16x9 Widescreen with 18 MHz Y sampling	1	1	0
PAL 4:4:4:4 Single Link with 13.5 MHz Y sampling	1	1	1

Both the GS9025 and GS9020 can also be configured for manual tune mode. To configure the GS9025 for manual mode, the A/$\overline{M}$ switch on SW1 must first be set LOW and then the appropriate standard selected via SS[2:0], also on SW1. Note that whenever the A/$\overline{M}$ input on the GS9025 is HIGH (auto mode), the SS[2:0] switches on SW1 must be in the VCC position to avoid bus contention. The GS9020 is configured for auto standards detect mode by default (power-on or reset). To configure it for manual standards detect, the STD[3:0], STD_SEL, and S bits of the HOSTIF write table must be set appropriately via the I²C interface.

The CD_ADJ input of the GS9025 is biased via a resistor network including a potentiometer allowing the user to adjust the level at which loss of carrier is detected. For a detailed description of the CD_ADJ voltage level versus muting threshold refer to the GS9025 data sheet. Turning the potentiometer completely counter-clockwise allows for maximum possible cable length equalization.

To verify operation of the EB9025/20, a source of serial digital video should be applied to the input BNC connector using 75Ω co-axial cable. Using a signal source that is not compliant to the SMPTE standards, can provide misleading results for equalizer cable length performance. The output data stream is available at the serial output and can be supplied to a D to A converter for verification via a monitor. Alternatively, the parallel output can be supplied to a TTL to ECL converter module and then to a D to A converter. Note that the following configuration signals must be set as shown for an output to be present:

A/$\overline{M}$ = HIGH (auto tune mode on GS9025)
A/$\overline{D}$ = HIGH (analog input select on GS9025)
SMPTE = HIGH (SMPTE mode select on GS9025)
$\overline{BLANK\_EN}$ = HIGH (blanking disabled on GS9020)
SDOMODE = HIGH (serial outputs enabled on GS9020)

PCB DETAILS

The EB9025/20 is a four layer printed circuit board constructed of standard FR-4 material and measures approximately 6" by 4". Ground and power plane layers are internal to the board with signal layers on the top and bottom of the board. Components are mounted on both the top and bottom sides. The silkscreen (top and bottom) and all four layers are shown on the following pages. Note the following special artwork features used to optimize performance:

- A continuous ground plane is provided underneath all high speed traces avoiding impedance discontinuities and ensuring maximum signal integrity

- The ground plane is isolated between the analog (GS9025) and digital (GS9020) areas of the board and flows directly to the power supply connection. Note that the isolation cut passes underneath the GS9020 ensuring that the high speed traces between the GS9025 and the GS9020 (serial clock and data) do not cross a ground plane discontinuity.

- The power plane is completely isolated between the analog (GS9025) and digital (GS9020) areas of the board.

- The GS9025 and the GS9020 are placed as close as possible to each other resulting in short trace lengths for the high speed serial data and clock signals and thus maximizing signal integrity.

- The serial data and clock lines from the GS9025 and GS9020 are symmetrical and equal in length resulting in equal propagation delay times.

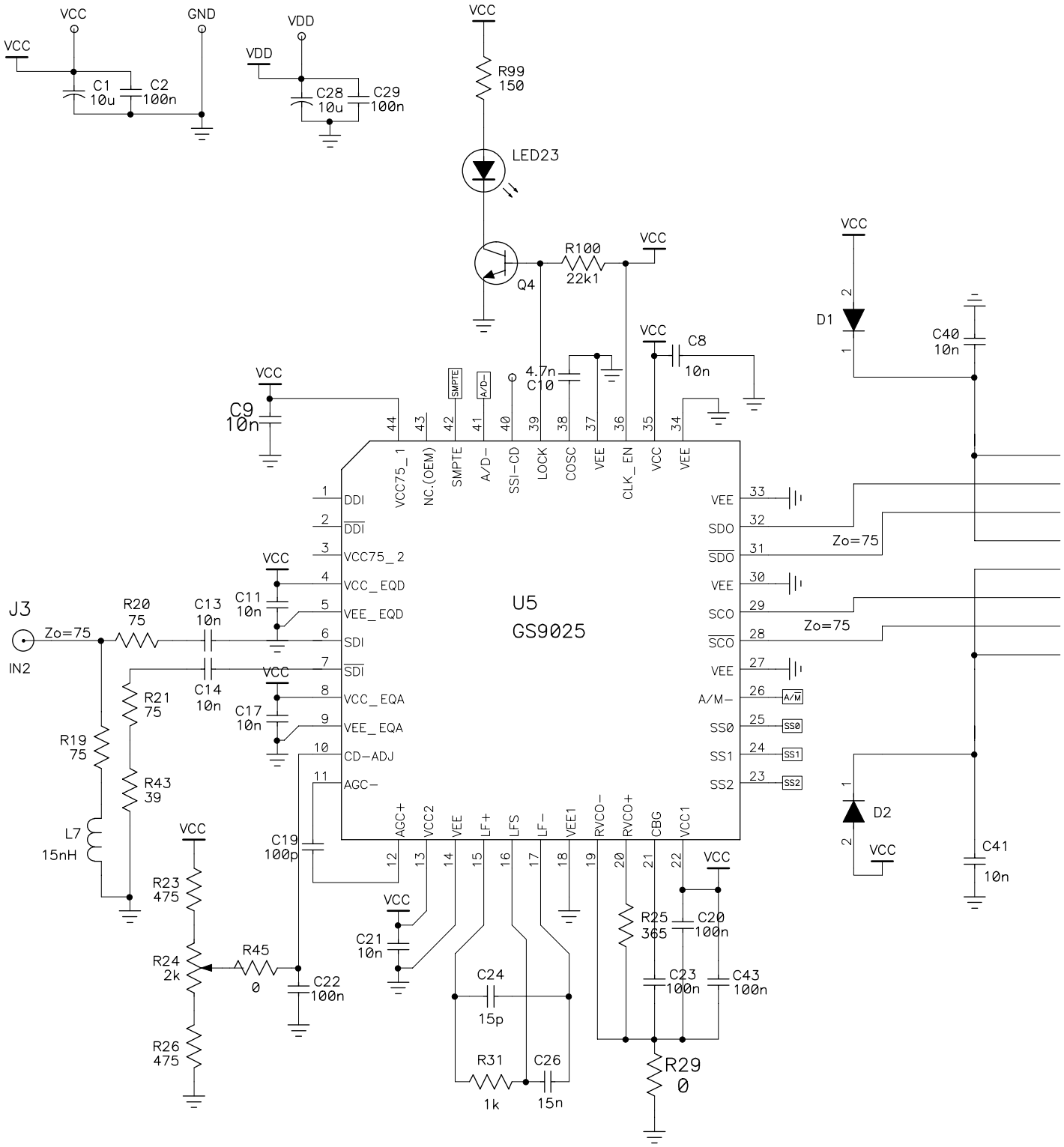
- Copper on the power and ground planes has been removed from underneath the output components of the GS9028 cable driver. The purpose of these cutouts is to reduce the effect of the capacitance added by the pads of the components.

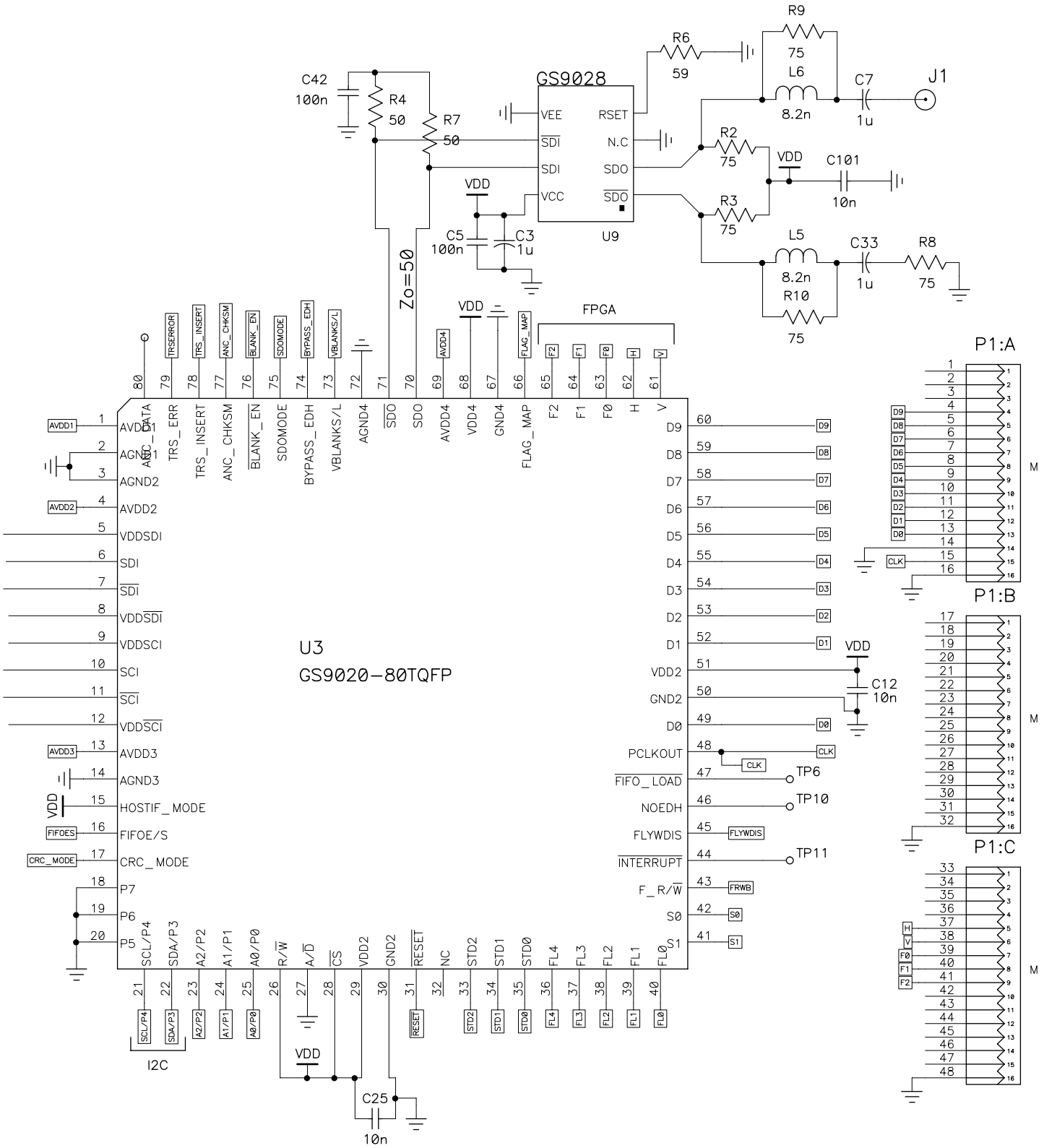
- Copper on the power and ground planes has been removed from underneath the loop filter and RVCO components of the GS9025. The purpose of these cutouts is to avoid any noise coupling from the planes into the GS9025.

APPLICATIONS

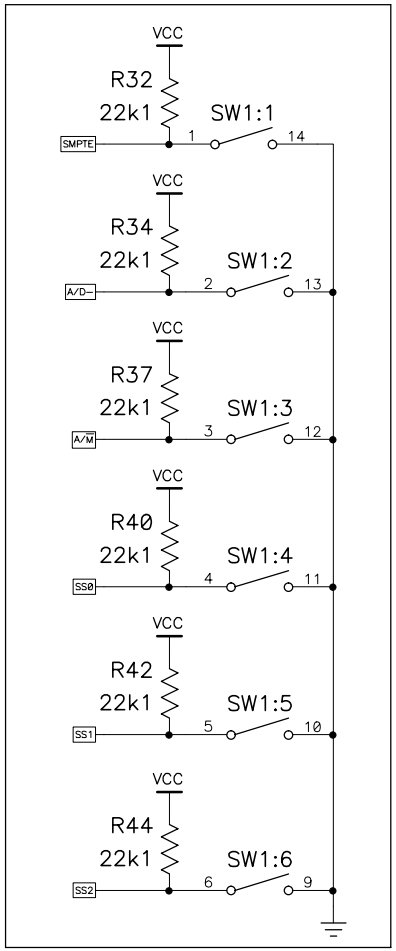
The EB9025/20 evaluation board is designed to show the characteristics of the GS9025 Receiver, the GS9020 Input Processor, and the GS9028 Cable Driver. This board can also be used as a stand alone serial to parallel converter with EDH processing as well as a reclocking distribution amplifier for serial digital video interfaces.

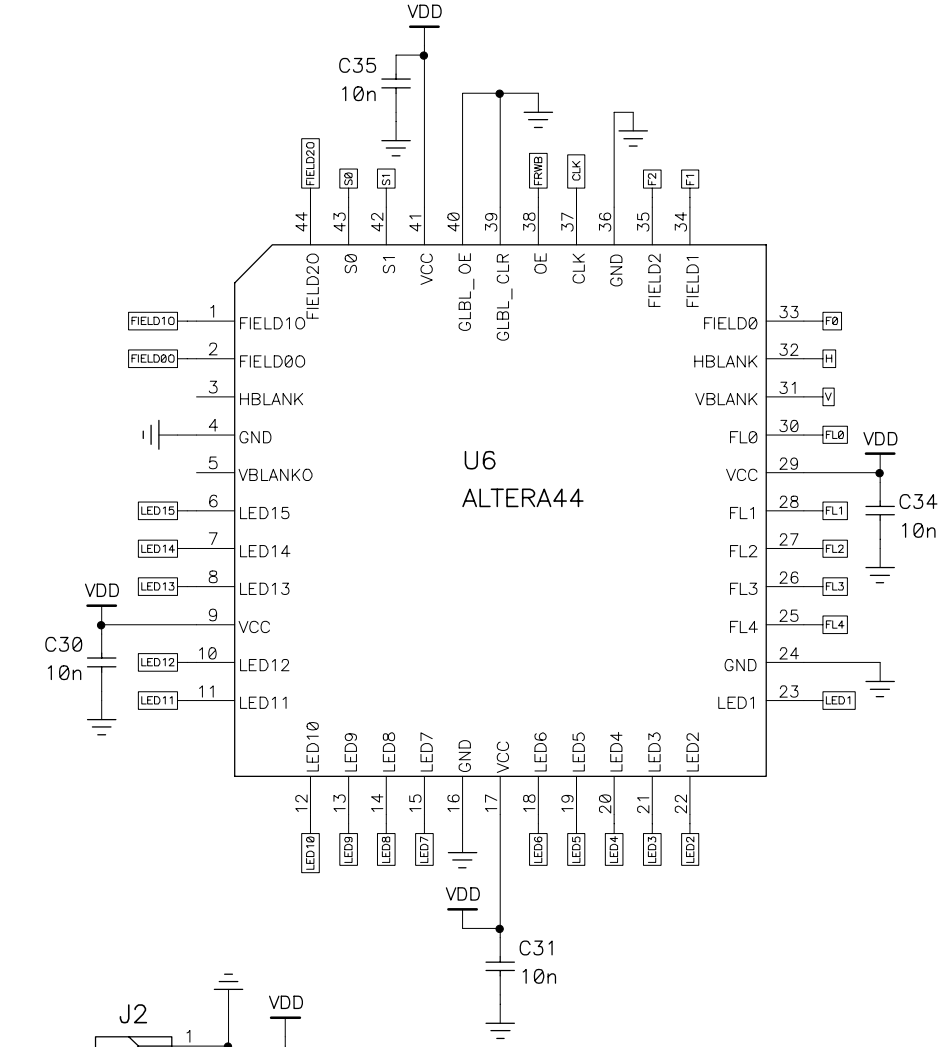
CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE

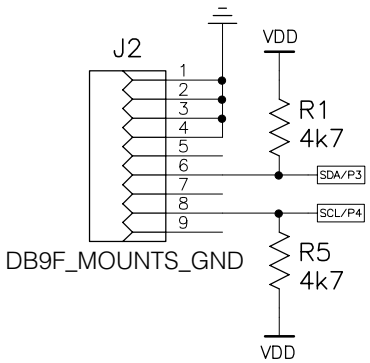

VCC
GND
C1
10u
C2
100n
VDD
C28
10u
C29
100n
R99
150
LED23
Q4
R100
22k1
4.7n
C10
C8
10n
C9
10n
D1
C40
10n
U5
GS9025
VCC75_1
NC.(OEM)
SMPTE
A/D–
SSI–CD
LOCK
COSC
VEE
CLK_EN
VCC
VEE
DDI
DDI
VCC75_2
VCC_EQD
VEE_EQD
SDI
SDI
VCC_EQA
VEE_EQA
CD–ADJ
AGC–
VEE
SDO
SDO
VEE
SCO
SCO
VEE
A/M–
SS0
SS1
SS2
Zo=75
Zo=75
J3
Zo=75
IN2
R20
75
C13
10n
C11
10n
C14
10n
C17
10n
R21
75
R19
75
R43
39
L7
15nH
C19
100p
R23
475
R24
2k
R45
0
C22
100n
R26
475
C21
10n
C24
15p
R31
1k
C26
15n
R25
365
C20
100n
C23
100n
C43
100n
R29
0
D2
C41
10n

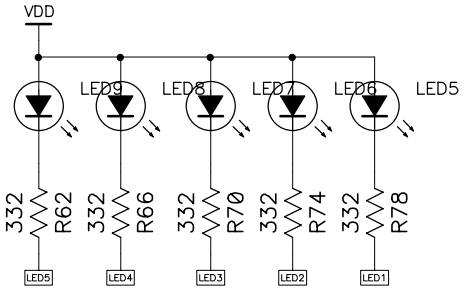

GS9028
U9
VEE
RSET
SDI
N.C
SDI
SDO
VCC
SDO
C42
100n
R4
50
R7
50
R6
59
R9
75
L6
8.2n
C7
1u
J1
R2
75
VDD
C101
10n
R3
75
C5
100n
C3
1u
L5
8.2n
R10
75
C33
1u
R8
75
Zo=50
FPGA
U3
GS9020–80TQFP
P1:A
P1:B
P1:C
C12
10n
C25
10n
I2C
TP6
TP10
TP11

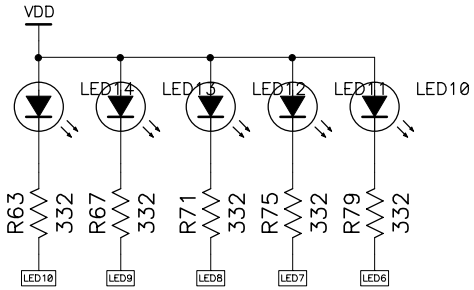
Switches for 9025

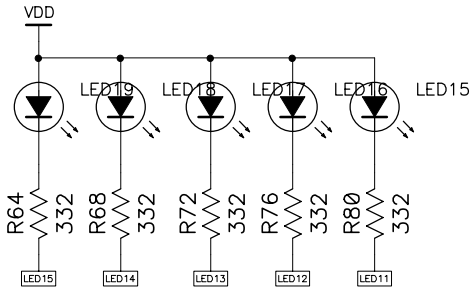


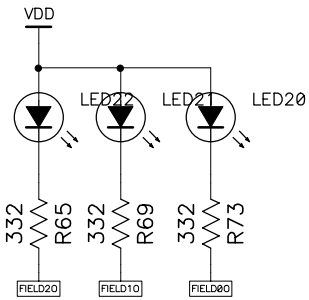




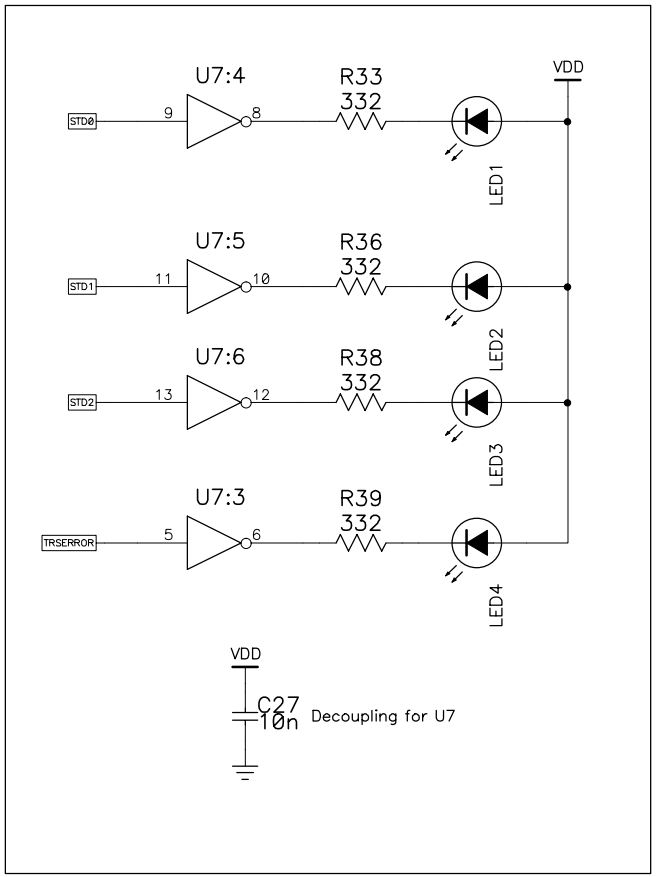




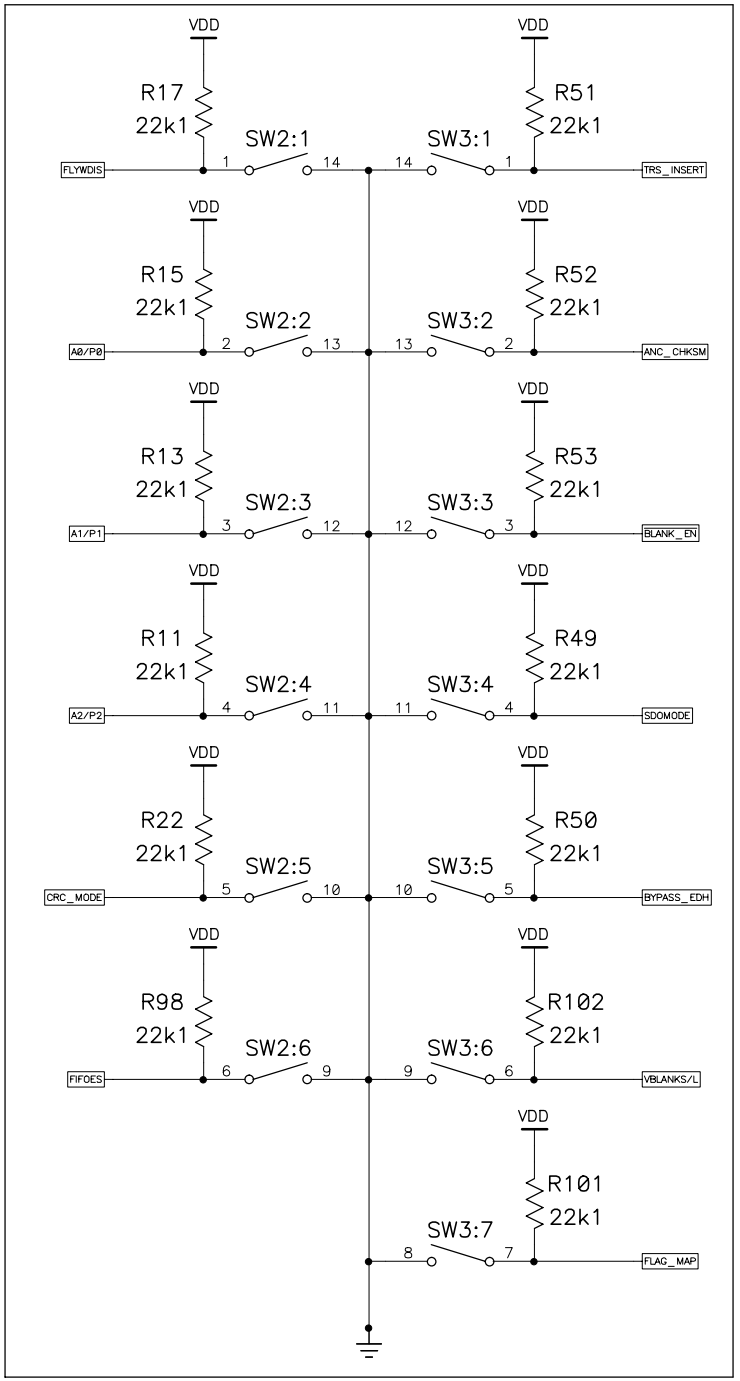




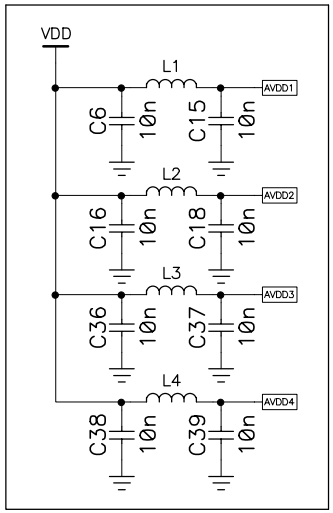
LEDs for 9020

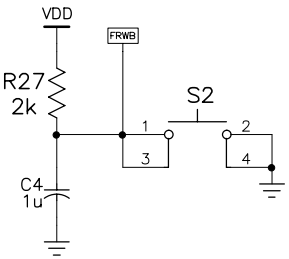


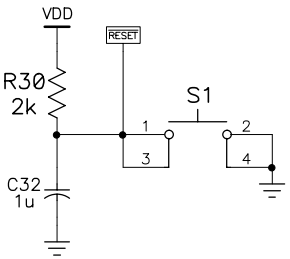
Switches for 9020



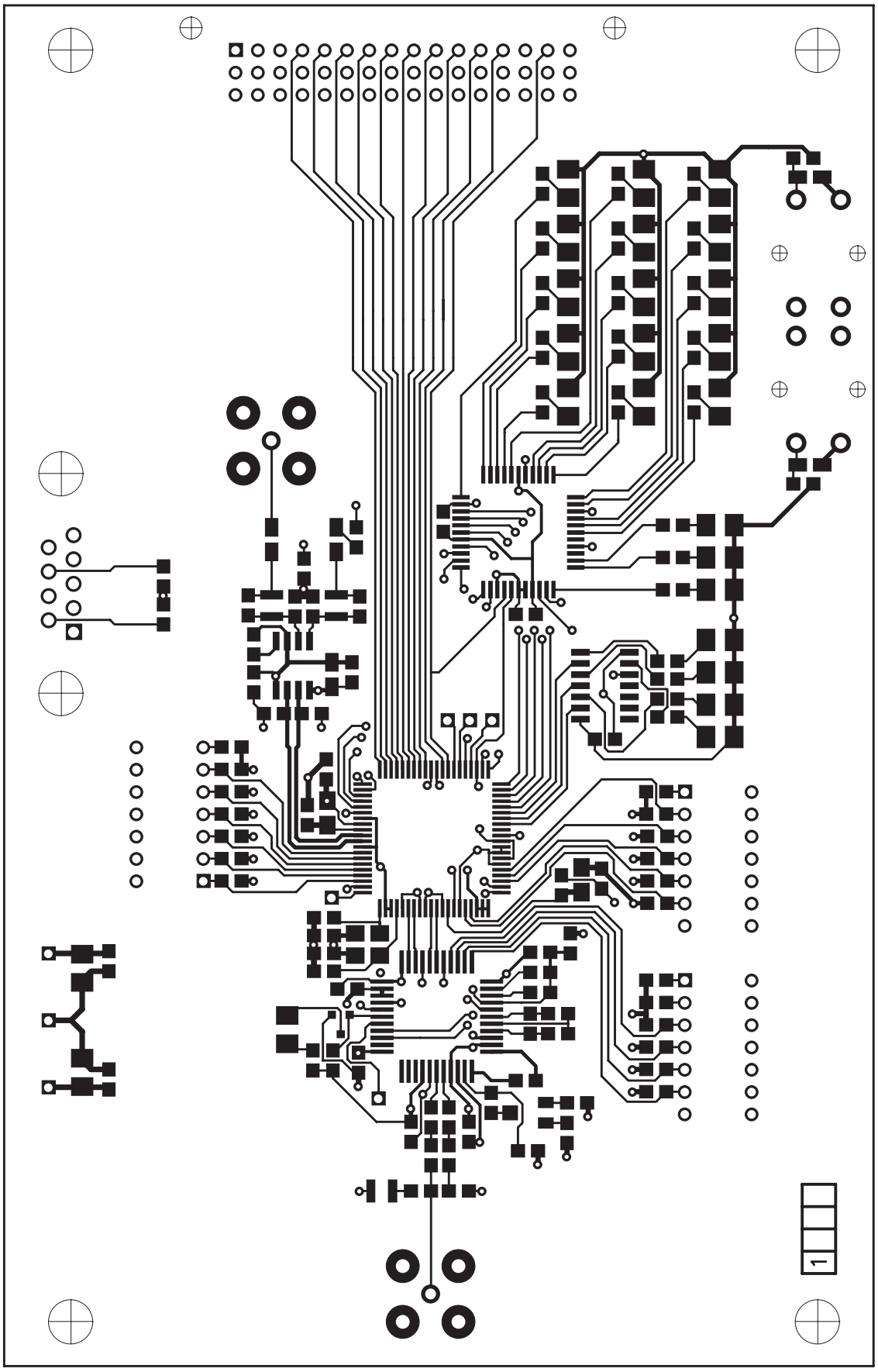
Filters

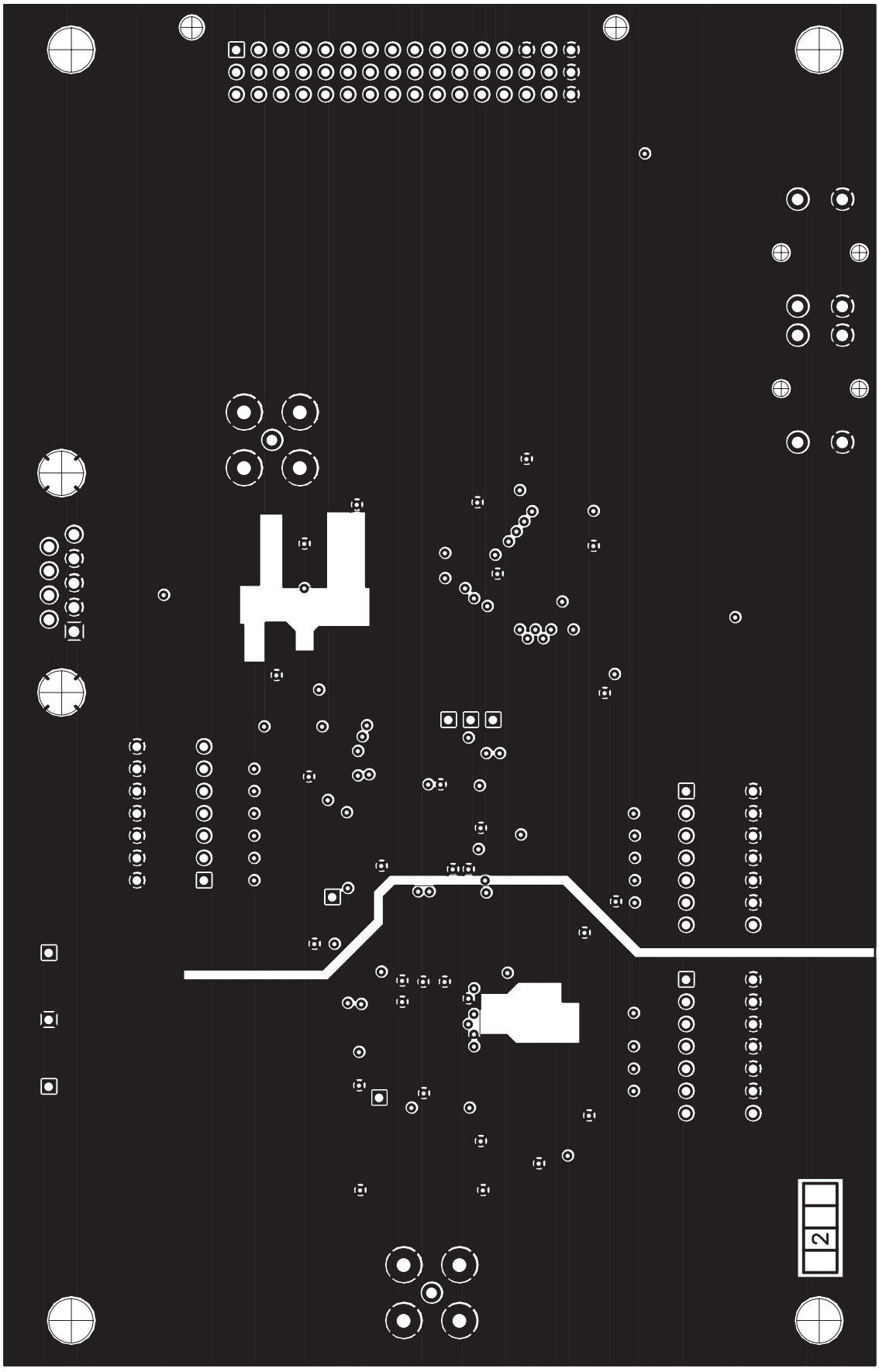


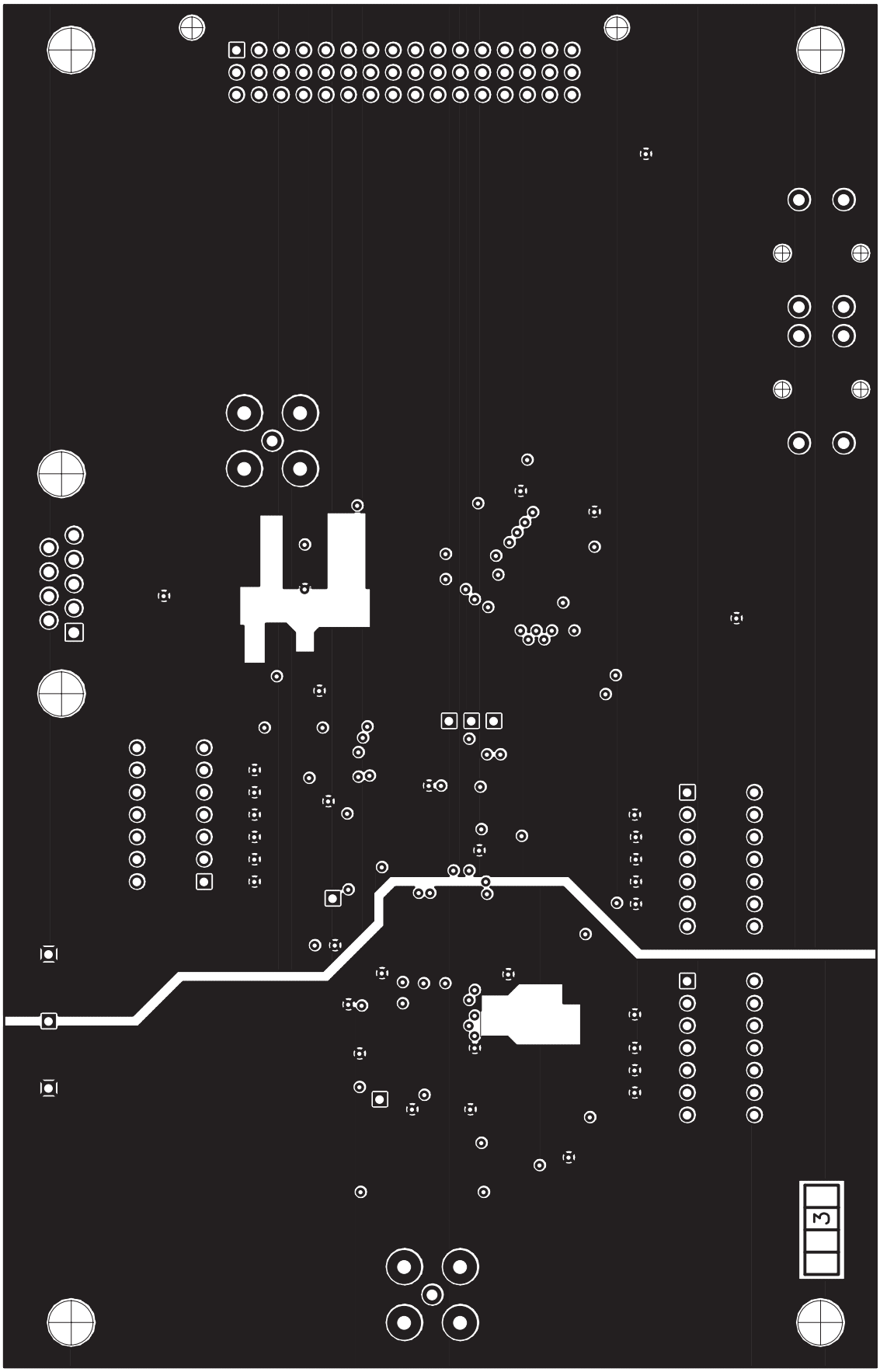


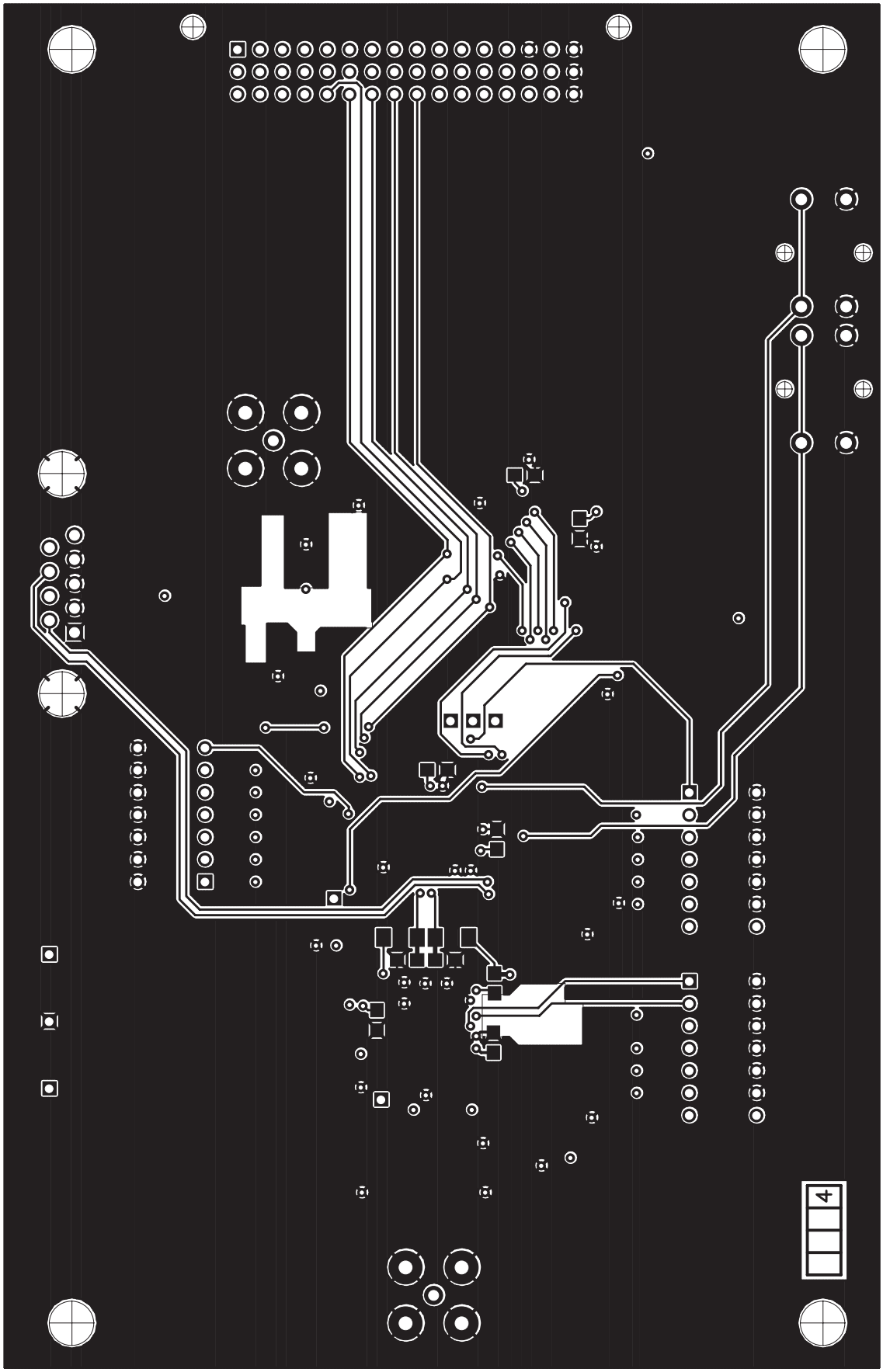


EB9025/20
GENLINX™ II
SERIAL TO PARALLEL
CONVERSION
REV 1.1
GENNUM
CORPORATION
MALE
BOARD EDGE
Serial Out
I²C Interface
SIN
SSI/CD
LOCK
ANC DATA
VCC
GND
VDD
SW1
SW2
SW3
AP
FF
ANC
UES IDA IDH EDA EDH
RESET
INC. FLAGS
FIFO_LOAD
NO_EDH
INTERRUPT
TRS_ERROR
STD0
STD1
STD2
F0
F1
F2
FIFOE/SI
CRC_MODE
A2/P2
A1/P1
A0/P0
FLYWDIS
SMPTE
A/D
A/M
SS0
SS1
SS2
CLIP_TRS
ANC_CHKSM
BLANK_EN
SDOMODE
BYPASS_EDH
VBLANKS/L
FLAG_MAP


1


2


3


4